UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,402	06/23/2003	Robert E. Cypher	5181-99401	7791

35690 7590 11/28/2005

MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL, P.C.
P.O. BOX 398
AUSTIN, TX 78767-0398

EXAMINER	
DILLER, JESSE DAVID	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/601,402	CYPHER ET AL.	
	Examiner	Art Unit	
	Jesse Diller	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/136,619.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/13/04, 1/25/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are pending in the application, and have been examined.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 10/136,619, filed on May 1, 2002.

Specification

3. The disclosure is objected to because of the following informalities: On Page 12, line 30, after "a service processor coupled to," "switch 250" should be replaced by "mode unit 250."

Appropriate correction is required.

Information Disclosure Statement

4. The Information Disclosure Statements filed 5/13/2004 and 1/25/2005 have been considered by the Examiner.

5. As required by **M.P.E.P. § 2001.06(b)** and **37 C.F.R. 1.98(d)**, since the instant application has been identified as a continuation application of an earlier filed application and is relied upon for an earlier filing date under **35 U.S.C. 120**, the examiner has reviewed the prior art cited in the earlier related application as required by **M.P.E.P. 707.05** and **904** and as stated in **M.P.E.P. 2001.06(b),** no separate citation of the same prior art need be made by the applicants in the instant application.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. **Claim 1 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 5 of copending Application No. 10,136,619.**

7. Initially, it should be noted that the present application is a continuation-in-part of Application No. 10,136,619, and has the same inventive entity. The assignee for both applications is Sun Microsystems.

8. Claimed subject matter in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that

copending application since the referenced copending application and the instant application are claiming common subject matter, as follows:

9. Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other copending application. See MPEP § 804.

10. Claim 1 is compared to claim 5 of application 10,388,193 in the following table:

Instant Application	Application 10/136,619
A multiprocessing system comprising:	A multiprocessing system comprising a plurality of clients; wherein
a plurality of	at least two of the plurality of clients comprise
processing subsystems, each including a cache memory;	processing subsystems, each including a cache memory;
	and wherein at least one of the plurality of clients comprises
a memory subsystem including a directory;	a memory subsystem including a directory;
a network	and a network separate from said clients', wherein said network includes a switch comprising a plurality of ports, wherein
interconnecting said plurality of processing subsystems and said memory subsystem;	each of said plurality of clients may be coupled to a respective one of said plurality of ports,

Instant Application	Application 10/136,619
	wherein the switch is configured to: receive a first coherency request from a given client, wherein said first coherency request is not visible to any other of said plurality of clients', and transmit a second coherency request in response to receiving said first coherency request;
wherein the network includes a mode unit configured to control whether a given coherency request is transmitted through said network according to a directory protocol or a broadcast protocol, and wherein	wherein the switch further comprises a coherency mode storage unit configured to store an indication to control whether the switch will transmit said second coherency request according to a directory protocol or a broadcast protocol:
	wherein if said second coherency request is transmitted by said switch according to said directory protocol: said second coherency request is transmitted by said switch to only said client comprising said memory subsystem'. said directory is accessed by said memory subsystem'. and responsive coherency commands are provided to one or more of said plurality of processing subsystems dependent upon information contained within said directory; (claim 1)
said given coherency request is initiated by a requesting processing subsystem, and wherein an encoding of said given coherency request excludes an indication of whether said given coherence request is to be transmitted according to said directory or broadcast protocols. (claim 1)	said first coherency request is initiated and transmitted from a requesting processing subsystem through a point-to- point link; and does not specify whether said second coherency request is transmitted by said switch according to said directory protocol or said broadcast protocol.(claim 5)

11. This is a provisional double patenting rejection since the conflicting claims have not yet been patented. The double patenting rejection is also applicable to other claims in the application, for instance, claims 13-17.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. **Claims 1-4, 7-10, 12-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Hagersten, US 5,864,671**.

14. **As for claims 1, 12-13, 16, Hagersten teaches**:

- A multiprocessing system including (slave nodes, 512, Fig. 5 each include processor, cache, memory, and directory 700-704, 950, of Fig. 10);
- a plurality of processing subsystems, each including a cache memory (700+702, Fig. 10);
- a memory subsystem including a directory (708, 950, Fig. 10; each slave node includes a memory subsystem with a directory); and
- a network interconnecting the clients (12, Fig. 1 + 206,600, Fig. 6 at home node);
- wherein said network includes a mode unit configured to control whether the network will transmit a coherency request according to a directory protocol or a broadcast protocol (partial directory cache at home node stores indications which control which protocol is used; see Fig. 11, also Col. 13, lines 47-60);
- Said given coherency request is initiated by a requesting processing subsystem (Col. 8, lines 61-63).

- The coherency request does not specify whether it is transmitted according to said directory protocol or said broadcast protocol (the requestor is not aware of the protocol; the protocol determination is made by the switch at the home node; i.e., transparently; see also Fig. 11).

15. **As for claim 2, Hagersten teaches**:

- The directory includes a plurality of entries corresponding to different memory locations mapped to said memory subsystem wherein each entry contains information indicative of whether a cached copy of a corresponding block has been created in one or more of said plurality of processing subsystems (See Figs. 4, 6; also Col. 2, line 64 to Col. 3, line 8).

16. **As for claim 3, Hagersten teaches**:

- The multiprocessing system as recited in Claim 2 wherein when said given coherency request is transmitted through said network according to said broadcast protocol, said coherency request is broadcasted to said memory subsystem and to each of said plurality of processing subsystems regardless of information contained within said directory (Col. 2, lines 13-15; this is the definition of 'broadcast': the request is broadcasted to "all the nodes in the network" without checking the directory; see Col. 9, lines 11-15 and Col. 13, lines 53-60).

17. **As for claim 4, Hagersten teaches**:

- Said given coherency request is initiated and transmitted through a point-to-point link (See Col. 1, lines 35-40; the network may be **any** configuration and protocol; this includes point-to-point configuration).

18. **As for claims 7, 14, 17 Hagersten teaches**:

- a coherency mode storage unit configured to store an indication to control whether the switch will transmit said coherency request according to a directory protocol or a broadcast protocol (partial directory cache at home node stores indications which control which protocol is used; see Fig. 11, also Col. 13, lines 47-60).

19. **As for claim 8, 18, Hagersten teaches**:

- the coherency mode storage unit stores a plurality of *additional indications* to control which protocol should be used (Col. 18, lines 22-48, Col. 17, lines 58-62).

20. **As for claim 9, 19, Hagersten teaches**:

- selected coherency requests are transmitted through the network by a directory protocol, and other coherency requests are transmitted through the network by a broadcast protocol. (the selection of which requests are transmitted by which protocol is based on the indication from the mode storage directory cache at the home node; See Fig. 11)

21. **As for claim 10, 20, Hagersten teaches**:

- An address of the first coherency request is used to dictate whether the second coherency request is transmitted through said network according to said directory protocol or said broadcast protocol (the address of the coherency request is used

to reference the directory; See Fig. 6; the ADDR is used to reference the directory entries)

22. **As for claim 15, Hagersten teaches**:

- Accessing a directory entry in response to said coherency request when said coherency request is transmitted through said network according to said directory protocol (1106, Fig. 11; Col. 9, lines 1-7).

23. **Claims 1-7, 13-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Martin, US 2002/0133674 A1.**

24. **As for claims 1,7, 13, 16, Martin teaches**:

- A multiprocessing system (Pg. 3, Par. 44, line 1) comprising:
- A plurality of processing subsystems (12a-f, Fig. 1; Pg. 3, Par. 44, line 2-3), each including a cache memory (22, Fig. 1; Pg. 3, Par. 45, line 2);
- A memory subsystem (16, Fig. 1; Pg. 3, Par. 44, lines 8-9) including a directory (21, Fig. 1; Pg. 3, Par. 44, line 10);
- A network interconnecting said plurality of processing subsystems and said memory subsystem (14, Fig. 1; Pg. 3, Par. 44, line 3)
- A coherency mode unit (26, Fig. 1) configured to store an indication (42, Fig. 4; see also Pg. 3, Par. 57) to control whether a given coherency request is transmitted through said network according to a directory protocol or a broadcast protocol (Pg. 3, Par. 52). (While Martin does not name this unit a coherency

mode storage unit, the cache controller he discloses performs the function of the mode unit disclosed by the instant application.)

- Said given coherency request is initiated by a requesting processing subsystem, (Claim 1(a) teaches initiation from a processor)
- and wherein an encoding of said given coherency request excludes an indication of whether said given coherence request is to be transmitted according to said directory protocol or said broadcast protocol (Page 4, Par. 61, lines 4-6 teach that the protocol indication is determined by circuitry hardwired into the memory controller, not programmed into a request; i.e., the protocol is transparent to the requesting subsystem).

25. **As for claim 2, Martin teaches**:

- The directory (21, Fig. 1; Pg. 3, Par. 44, line 10) includes a plurality of entries corresponding to different memory locations mapped to said memory subsystem (Pg. 3, Par. 46, lines 4-6), wherein:
- Each entry contains information indicative of whether a cached copy of a corresponding block has been created in one or more of said plurality of processing subsystems (Pg. 3, Par. 46, lines 4-7).

26. **As for claim 3, Martin teaches**:

- When a coherency request is transmitted through said network (Pg. 3, Par. 47, lines 1-4) according to said broadcast protocol, said coherency request is broadcasted to said memory subsystem and to each of said plurality of

processing subsystems regardless of information contained within said directory (Pg. 3, Par. 50, lines 1-3, 5-10).

27. **As for claim 4, Martin teaches**:

- Said given coherency request is initiated by a requesting processing subsystem, and wherein said given coherency request is transmitted to said network through a point-to-point link (Claim 1(a) teaches initiation from a processor unit and that the request is transmitted directly from one PU to another, i.e., point-to-point network. Also see Fig. 1 for PTP connection between PU 12a and network 14).

28. **As for claims 5-6, 15, Martin teaches**:

- That when said coherency request is transmitted through said network according to said directory protocol (Page 3, Par. 51, lines 1-3),
- Said given coherency request is transmitted through said network to said memory subsystem. (Page 3, Par. 51, line 3 teaches that the request is transmitted to the directory; Pg 2, Par. 44, lines 8-10 teach that the directory is included in the memory subsystem),
- An entry in said directory is accessed by said memory subsystem (Page 3, Par. 51, lines 4-7), and
- Responsive coherency commands are provided to one or more of said plurality of processing subsystems dependent upon information contained within said directory (Page 3, Par. 51, lines 8-10).

29. **As for claims 7, 14, and 17, Martin teaches**:

- A coherency mode storage unit (26, Fig. 1) configured to store an indication (42, Fig. 4; see also Pg. 3, Par. 57) to control whether a given coherency request is transmitted through said network according to a directory protocol or a broadcast protocol (Pg. 3, Par. 52); (While Martin does not name this unit a coherency mode storage unit, the cache controller he discloses performs the function of the mode unit disclosed by the instant application).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

30. Claims 8-10, 12, and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martin in view of Hagersten, US Patent 5,887,138.

31. As for the limitations of claims 8-10, Martin teaches all the limitations of claim 7 as described above in the section entitled *Claim Rejections – 35 USC § 102.* Martin additionally teaches that his mode storage unit stores an indication (42, Fig. 4) to control whether coherency requests are transmitted through the network by a broadcast protocol or by a directory protocol (Pg. 3, Par. 57; Pg. 3, Par. 52). He teaches that, based on the indication, selected coherency requests are transmitted through the network by a directory protocol, and other coherency requests are transmitted through the network by a broadcast protocol. (The limitation of claim 9 in the instant application)

32. Martin, however, does not expressly teach that the coherency mode storage unit stores a plurality of *additional indications* to control which protocol should be used nor that an address of the request is one of the indications used to dictate the transmission protocol, as is claimed in claims 8 and 10.

33. Hagersten, US Patent 5,887,138, does teach these limitations, disclosing a multiprocessing computer system which includes a plurality of processing units (16, Fig. 1) with individual caches (18, Fig. 1), a shared memory (22, Fig. 1; also 36, Fig. 1A and 46, Fig. 1B), a point to point network (14, Fig. 1; also Col. 7, line 10) connecting the components, and a system interface (i.e., mode storage unit) which determines the transmission protocol (24, Fig. 1; Fig. 3; Col. 5, lines 18-24). Hagersten's system uses multiple coherency protocols depending on several indications, including whether a coherency request is directed toward a local or global address. Hagersten discloses that his system interface uses several indications to determine the protocol used, namely:

- Whether the address is local or global (Col. 5, lines 21-25);
- Whether there is a copy of the requested memory block in additional local memories in other global units (Col. 5, lines 21-25); and
- The access rights of the unit in question. (Col. 16, lines 22-28)

34. Hagersten discloses that his system interface stores:

- Translations from local to physical addresses, comparing several bits from the requested address to information stored in the interface (Col. 13, line 59 to Col. 14, line 3); and

- Information in an MTAG table (68, Fig. 3) that is used to determine access rights.

These indications are used in the determination of the protocol (Col. 16, lines 10-25).

35. Martin and Hagersten are analogous art because they are from the same field of endeavor, namely multiprocessing systems that use multiple and differing coherency protocols based on certain situations in an effort to reduce request latency and reduce network congestion.

36. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Martin to include the storage of multiple indications for protocol differentiation based on local / global address.

37. The suggestion for doing so is taught by Hagersten, on Col. 4, lines 20-50. The distributed memory architecture format sometimes used for multiprocessor systems can cause network congestion, creating a bottleneck. When a processor accesses a portion of memory that is not local to the processor's own node, it must create some network traffic. As lines 32-40 note, coherence requests directed to a shared memory segment local to the processor's own node operate at a much higher bandwidth than requests directed over the network to a memory segment that is not local. Therefore, it would have been obvious to try to find a way to decrease the disadvantage that non-local coherence requests experience. A logical conclusion would be that the protocols that work well for local requests might not work well for non-local requests, because they create a bandwidth problem. Martin, in Page 1, Par. 7, notes that certain protocols that work quickly for small systems are not as desirable for large systems because they

create a lot of network traffic, and that other protocols, while slower and more complex, (lines 3-4) use less bandwidth and would be better for use in non-local requests sent over a network.

38. Therefore it would have been obvious to modify the system of Martin by adding the limitations of Hagersten described above to create a system that has the advantage of quick request completion for both local addresses and non-local addresses, to obtain the invention as specified in claims 8-10.

39. As for the limitations of claims 18-20, Martin teaches all the limitations of claim 17 as described above in the section entitled *Claim Rejections – 35 USC § 102.* Martin additionally teaches that his mode storage unit stores an indication (42, Fig. 4) to control whether coherency requests are transmitted through the network by a broadcast protocol or by a directory protocol (Pg. 3, Par. 57; Pg. 3, Par. 52). He teaches that, based on the indication, selected coherency requests are transmitted through the network by a directory protocol, and other coherency requests are transmitted through the network by a broadcast protocol. (The limitation of claim 19 in the instant application)

40. Martin, however, does not expressly teach that the coherency mode storage unit stores a plurality of *additional indications* to control which protocol should be used nor that an address of the request is one of the indications used to dictate the transmission protocol, as is claimed in claims 18 and 20.

41. **Hagersten, US Patent 5,887,138**, does teach these limitations, disclosing a multiprocessing computer system which includes a plurality of processing units (16, Fig.

1) with individual caches (18, Fig. 1), a shared memory (22, Fig. 1; also 36, Fig. 1A and 46, Fig. 1B), a point to point network (14, Fig. 1; also Col. 7, line 10) connecting the components, and a system interface (i.e., mode storage unit) which determines the transmission protocol (24, Fig. 1; Fig. 3; Col. 5, lines 18-24). Hagersten's system uses multiple coherency protocols depending on several indications, including whether a coherency request is directed toward a local or global address. Hagersten discloses that his system interface uses several indications to determine the protocol used, namely:

- Whether the address is local or global (Col. 5, lines 21-25);
- Whether there is a copy of the requested memory block in additional local memories in other global units (Col. 5, lines 21-25); and
- The access rights of the unit in question. (Col. 16, lines 22-28)

42. Hagersten discloses that his system interface stores:

- Translations from local to physical addresses, comparing several bits from the requested address to information stored in the interface (Col. 13, line 59 to Col. 14, line 3); and
- Information in an MTAG table (68, Fig. 3) that is used to determine access rights.

43. These indications are used in the determination of the protocol to be used (Col. 16, lines 10-25)

44. Martin and Hagersten are analogous art because they are from the same field of endeavor, namely multiprocessing systems that use multiple and differing coherency

protocols based on certain situations in an effort to reduce request latency and reduce network congestion.

45. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Martin to include the storage of multiple indications for protocol differentiation based on local / global address.

46. The suggestion for doing so is taught by Hagersten, on Col. 4, lines 20-50. The distributed memory architecture format sometimes used for multiprocessor systems can cause network congestion, creating a bottleneck. When a processor accesses a portion of memory that is not local to the processor's own node, it must create some network traffic. As lines 32-40 note, coherence requests directed to a shared memory segment local to the processor's own node operate at a much higher bandwidth than requests directed over the network to a memory segment that is not local. Therefore, it would have been obvious to try to find a way to decrease the disadvantage that non-local coherence requests experience. A logical conclusion would be that the protocols that work well for local requests might not work well for non-local requests, because they create a bandwidth problem. Martin, in Page 1, Par. 7, notes that certain protocols that work quickly for small systems are not as desirable for large systems because they create a lot of network traffic, and that other protocols, while slower and more complex, (lines 3-4) use less bandwidth and would be better for use in non-local requests sent over a network.

47. Therefore it would have been obvious to modify the system of Martin by adding the limitations of Hagersten described above to create a system that has the advantage

of quick request completion for both local addresses and non-local addresses, to obtain the invention as specified in claims 18-20.

48. **As for claim 12**, Martin teaches

- A multiprocessing system (Pg. 3, Par. 44, line 1) comprising:
- A memory subsystem (16, Fig. 1; Pg. 3, Par. 44, lines 8-9) including a directory (21, Fig. 1; Pg. 3, Par. 44, line 10), the directory (21, Fig. 1; Pg. 3, Par. 44, line 10) including a plurality of entries corresponding to different memory locations mapped to said memory subsystem (Pg. 3, Par. 46, lines 4-6);
- A plurality of processing subsystems (12a-f, Fig. 1; Pg. 3, Par. 44, line 2-3), each including a cache memory (22, Fig. 1; Pg. 3, Par. 45, line 2);
- A network interconnecting said plurality of processing subsystems and said memory subsystem (14, Fig. 1; Pg. 3, Par. 44, line 3)
- A coherency mode unit (26, Fig. 1) configured to control whether a given coherency request is transmitted through said network according to a directory protocol or a broadcast protocol (Pg. 3, Par. 52). (While Martin does not name this unit a coherency mode storage unit, the cache controller he discloses performs the function of the mode unit disclosed by the instant application. It should also be noted that "point-to-point mode" has been taken to mean "directory mode.")
- Wherein the network is configured to route a coherency request for said given block initiated by one of said processing subsystems (Claim 1(a)) to said directory (Page 3, Par. 51, line 3) or to broadcast said coherency request to said

memory subsystem and to each of said plurality of processing subsystems (Pg. 3, Par. 50, lines 1-3, 5-10) in response to said indication.

- (Page 4, Par. 61, lines 4-6 teach that the protocol is determined by circuitry hardwired into the memory controller, not programmed into a request; i.e., the protocol is transparent to the requesting subsystem, which simply makes the request).

49. Martin does not expressly teach that the indication is to whether a given block is a directory mode block or a broadcast mode block, (i.e., that a block has a mode associated with it) or that these indications are the basis of the protocol choice, as does claim 12.

50. **Hagersten, US Patent 5,887,138, does teach these limitations,** disclosing a multiprocessing computer system which includes a plurality of processing units (16, Fig. 1) with individual caches (18, Fig. 1), a shared memory (22, Fig. 1; also 36, Fig. 1A and 46, Fig. 1B), a point to point network (14, Fig. 1; also Col. 7, line 10) connecting the components, and a system interface (i.e., mode storage unit) which determines the transmission protocol (24, Fig. 1; Fig. 3; Col. 5, lines 18-24). Hagersten's system uses multiple coherency protocols depending on several indications, including whether a coherency request is directed toward a local or global address. Hagersten discloses that his system interface uses several indications to determine the protocol used, including whether the address is local or global (Col. 5, lines 21-25). This indication is used in the determination of the protocol to be used (Col. 16, lines 10-25).

51. Hagersten uses one protocol for local addresses and another for global addresses (Col. 5, lines 20-23). Because the address range defined by a local memory is fixed, blocks of memory corresponding to local or global address ranges will always be accessed (by the same processor) using the same protocol. Therefore, blocks of memory could be said to be associated with the access protocol used to access them.

52. Martin and Hagersten are analogous art because they are from the same field of endeavor, namely multiprocessing systems that use multiple and differing coherency protocols based on certain situations in an effort to reduce request latency and reduce network congestion.

53. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Martin to include the storage of indications for protocol differentiation based on local / global address.

54. The suggestion for doing so is taught by Hagersten, on Col. 4, lines 20-50. The distributed memory architecture format sometimes used for multiprocessor systems can cause network congestion, creating a bottleneck. When a processor accesses a portion of memory that is not local to the processor's own node, it must create some network traffic. As lines 32-40 note, coherence requests directed to a shared memory segment local to the processor's own node operate at a much higher bandwidth than requests directed over the network to a memory segment that is not local. Therefore, it would have been obvious to try to find a way to decrease the disadvantage that non-local coherence requests experience. A logical conclusion would be that the protocols that work well for local requests might not work well for non-local requests, because they

create a bandwidth problem. Martin, in Page 1, Par. 7, notes that certain protocols that work quickly for small systems are not as desirable for large systems because they create a lot of network traffic, and that other protocols, while slower and more complex, (lines 3-4) use less bandwidth and would be better for use in non-local requests sent over a network.

55. Therefore it would have been obvious to modify the system of Martin by adding the limitations of Hagersten described above to create a system that has the advantage of quick request completion for both local addresses and non-local addresses, to obtain the invention as specified in claim 12.

56. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Martin in view of Higuchi et al, US 5,774,731, hereinafter Higuchi.

57. Martin discloses the limitations of claim 1, as above.

58. Martin, however, does not expressly disclose that the network is implemented with a plurality of address switches.

59. Higuchi discloses a multiprocessing system, with the processing subsystems (2, Fig. 1A) interconnected via a network (1, Fig. 1A). The network of Higuchi is implemented with a plurality of address switches (see EX00-33, Fig. 2; also Col. 9, lines 60-67), thereby creating a point-to-point connection between the nodes.

60. Higuchi and Martin are analogous art because they are from the same area of endeavor, namely multiprocessing systems which utilize a point-to-point network to interconnect processing subsystems.

61. At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the network of Higuchi in the system of Martin.

62. The motivation for doing so is disclosed by US 5,822,605 to Higuchi et al., (hereinafter "the '605 patent"), which is incorporated by reference in Higuchi's '731 patent. In Col. 4, lines 30-55 of the '605 patent, it is taught that the network allows rapid message transfer while avoiding deadlock, which is advantageous.

63. Therefore, it would have been obvious to combine Higuchi with Martin for the benefit of avoiding deadlock, to obtain the invention as specified in claim 11.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Phelps, US 5,966,729, discloses a multiprocessor system which includes both broadcast and directory coherence requests. The system includes a switch connecting the clients, and a central mode directory determining the transmission protocol.

Khare, US 6,810,467, teaches a multinode coherence system which includes a central switching device with a plurality of ports, to which the nodes are coupled.

Quatch, US 2004/0117561 A1, discloses a multi-client system with a centrol coherence switch. The switch receives point-to-point coherence requests from the clients and issues second requests based on a mode filter which acts as a directory. A further indication changes the mode so that the second requests are issued under a broadcast protocol instead of a directory protocol.

Deneroff, US 2005/0053057 A1, discloses a multi-nodal coherence system with a central network switch with individual ports. Coherence requests are routed from node to node, with the individual nodes not able to snoop the network.

For further applicable art, see the enclosed PTO-892 form.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse Diller whose telephone number is (571) 272-4173. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JD

DONALD SPARKS
SUPERVISORY PATENT EXAMINER